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Re: EMRS 2008 Symposium J

Title: Low Power, GHz Class ADC for Broadband Applications

Dear Sir,

I would be grateful if you could referee the attached paper for publication in the special issue of Materials Science in Semiconductor Processing for the proceedings of EMRS 2008 Symposium J.

Yours Faithfully,

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Low Power, GHz Class ADC for Broadband Applications

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Abstract— **The design of ultra low power (<100mW), high-speed analogue to digital converter (ADC) is an essential element for the next generation radio telescope, the square kilometre array (SKA). CMOS technology is limited in high precision applications, such as ADCs due to the stringent requirement of device matching. Also to achieve high-speed (f_T > 100GHz) CMOS requires deep sub-micron gates (90nm or less) where expensive phase shift masks are required. This paper describes the design and simulation of a low-power high-speed (4GS/s) analogue to digital converter (ADC) based on an InP/InGaAs heterojunction bipolar transistor (HBT). The technology used was developed at the University of Manchester using MBE growth which relied upon two novel developments. Firstly stoichiometric conditions permitted growth at a fairly low temperature of 420^{o}C while conserving extremely high quality materials. Secondly dimeric phosphorus was generated from a gallium phosphide (GaP) decomposition source leading to excellent rf device properties. The DC and RF performance of the fabricated HBTs showed characteristics ideally suited to low-power IC designs, with current gain ~70, low offset voltages and achieving an f_t=91GHz and f_{max}=83GHz on a 1.5×5μm^2 emitter area device using fairly relaxed optical lithography.**

Keywords : Heterojunction bipolar transistor; Molecular Beam Epitaxy; Indium gallium arsenide; Indium Phosphide; Gallium Phosphide; Complementary-metal-oxide-semiconductor; Silicon Germanium; Analogue to digital converter; Square kilometre array

PACS Codes: 81.05.Ea, 84.30.-r, 84.40.Lj, 85.30.De, 85.40.Bh.

1. INTRODUCTION

The microelectronics industry has depended upon silicon as the core material since the 1970's [1]. Rapid scaling of transistor and interconnect dimensions has enabled increasing chip complexity and speed. In terms of latest generation of CMOS for example, the gate oxide thickness must be reduced to less than 1 nm [2]. However, this has a consequence of increasing the gate leakage current that can only be resolved if a high-k, low defect density material (other than SiO_2) is introduced [3]. Even with these enhancements, CMOS technologies are only expected to provide low-resolution circuits up to 10-20GHz [4]. Beyond this region (>40Ghz), SiGe or III-V compound semiconductor technologies are the only viable option [4].

In mixed-signal applications and high-speed logic design, closely matched devices are indispensable. The improved threshold voltage control of heterojunction bipolar transistors (HBT) compared to FET devices make these an ideal choice. The voltage control of the HBT is dependent upon the material bandgap rather than the processing dependent Schottky barrier and Fermi level [5]. HBTs are also beneficial in high dynamic range applications including analogue to digital converters (ADC) due to inherent high linearity and fundamentally lower 1/f noise [6].

For low-resolution, GHz class ADCs both technologies are feasible [7-13] and have found widespread applications in radar receivers [11], digital oscilloscopes [10] and millimetre arrays for radio astronomy [12]. The maximum sampling rate of these ADCs can be enhanced either by utilising time-interleaved techniques [8] or using a process that offers faster devices (e.g. III-V [7, 10]). However, material choice is also an important factor for low-power applications. While SiGe can be used for speeds approaching 77Ghz [4], its peak electron velocity occurs at a much higher electric field

than InGaAs [14]. Hence to achieve comparable high-speed operation, SiGe HBTs require larger bias voltages and thus results in increased power dissipation. Also the low bandgap InGaAs used in the base layer of InP/InGaAs or AlInAs/InGaAs HBTs reduce the turn-on voltage, and are thus more suited to low-power applications.

This paper presents the research into developing ultra-low power ADCs based on InP/InGaAs heterojunction bipolar transistors (HBTs) that can be integrated into the next generation radio telescope, SKA [15]. The ultimate aim is to fabricate a 4-bit ADC that operates at a sampling frequency of 4GHz, and dissipates less than 100mW.

2. MATERIAL GROWTH AND FABRICATION

The epitaxial layers of the fabricated HBTs were performed on a VG 90H solid source MBE system on Fe-doped semi-insulating (100) InP substrates. The system utilised an ultra high vacuum (UHV) chamber with a base pressure of $<10^{-10}$ Torr. Pyrolitic boron-nitride crucibles were used for the evaporation of gallium, arsenic, indium, silicon and beryllium. Phosphorus was generated from a GaP decomposition source whose operational aspects are described elsewhere [16]. The growth was performed at a relatively low temperature of ~420^{o}C and used stoichiometric conditions for both the arsenide and phosphide materials. This had the added beneficial effects of confining the high concentration Be-dopant used in the structures.

The epitaxial structure of self-aligned HBTs used for this study is shown in Table 1. ADC designs are based solely on the SHBT structure. To minimise power consumption a DHBT structure is currently under investigation which utilises a thinner base and collector structure to improve high frequency performance. The DHBT also benefits

from reduced collector-emitter offset voltage (<50mV), high breakdown >8V and lower output conductance.

3. TRANSISTOR CHARACTERISATION AND MODELLING

Simulated and measured common-emitter current-voltage (*I-V*) characteristics of an SHBT with an emitter area of $1.5\times5\mu m^2$ are shown in Fig. 1. Microwave S-parameters were measured on an HP8510C network analyser using on-wafer probing over the frequency range of 45 MHz to 110 GHz. Prior to current gain collapse (caused by self-heating and the Kirk effect) the current-gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) were extrapolated to be 91GHz and 83GHz respectively at I_C=3.6mA and V_{CE}=1V. Devices possess excellent I-V characteristics with common-emitter breakdown voltage (BV_{CEO}) of 4.5V at I_C=100μA. The soft breakdown of the SHBT is attributed to the weak field dependence of electron impact ionization coefficient in InGaAs at medium to low electric field.

Transistor parameters were extracted [17, 18] from the transistor for non-linear modelling in Agilent's ICCAP and Advanced Design System (ADS) software. This software includes the small-signal University of San Diego (UCSD) model (standard SPICE Gummel-Poon modified model) for the HBT [19].

4. COMPARATOR DESIGN

The comparator cell shown in Fig. 2 is based on the low-power design proposed by Hotta et al [20]. It consists of an input buffer, preamplifier, latching comparator and output buffer.

The main design objective was to maximise operational speed, without consuming excessive power or chip area. Since emitter couple logic (ECL) is used extensively for the differential amplifiers, it is thus important to prevent these from entering into saturation. If occurred, the resulting base charge would seriously compromise high-frequency performance. The supply rail voltage was therefore set to a minimum of 3V and this value was also consistent with the BV_{CEO} of the HBT.

The most important components of the cell are the pre-amplifier stage and the latching comparator. The latter is created via two cross-coupled differential pairs that can either sample or hold data depending on the switching clocks (clk_p and clk_n). Since the gain of this stage is notoriously low, the recovery time can be substantial. It is well understood that the operational speed of this latch is roughly proportional to its current consumption. However, an alternative method to improve overall performance is to amplify the input signal before being feed into the latching comparator (pre-amplification). In this configuration it can be possible to obtain the same performance, but at a much reduced power.

As stated previously, the speed of the latching comparator is determined mainly by its recovery time (t_r), which can be expressed by Eq. 1. [20].

$$t_r = C_L R_L \equiv C_L \cdot \frac{\Delta V_O}{I_L} \qquad (1)$$

where C_L is the collector load capacitance, R_L is the collector load resistance, I_L is the tail current and V_O is the output voltage swing. Thus to optimise the circuit for low power operation, it is desirable optimise all factors in equation 1.

For a digital system, the output swing must be larger than the thermal voltage (V_T) ~26mV. In this work we have designed a voltage swing of approximately 10 times V_T ~ 250mV to allow the comparator relatively high noise immunity. Simulations were then conducted on the latched comparator to decide on suitable load currents (Fig. 3). The dotted line represents the 4GHz clock duration of 125ps, and provides an upper limit for the recovery time. To reduce the impact of meta-stable states, and improve sensitivity, a maximum recovery time of 60ps was chosen, setting the tail current to be ~520μA.

To optimise the input signal response, the pre-amplifier was designed to have the same time constant as that of the latching comparator [20]. The gain of the pre-amplifier is set to 3.4. The simulated negative level clock triggered the output of the optimised comparator as shown in Fig. 4, and produced state-of-the-art power consumption of 10.8mW at 4GS/s. The circuit was also re-optimised for a 2GHz clock, providing power reductions by 20% to ~7.8mW.

The full flash 4-Bit ADC includes 15 comparators, 15 ExORs, 32 diodes and resistor ladder producing a total power consumption of 240mW for 2GHz clock and 290mW for a 4 GHz clock. These values compare favourably to the state-of-the-art in various technologies [21-23]. However in CMOS for example [21, 22], power dissipation is proportional to the sampling frequency f_s, which can provide an upper limit for ultra low power designs.

5. ULTRA LOW POWER DESIGNS

There are a number of techniques for reducing power consumption.

A. Device performance

The low collector-emitter offset (V_{CEO}) in DHBT (<50mV) as compared to SHBT (~0.26V) offers a great advantage in reducing the power dissipation as shown in Fig. 5. Moreover the improved transconducatance, high breakdown voltage due to low impact ionization and high early voltage make DHBT more favourable for high speed low power applications.

B. Folding Flash ADC

The aim is to reduce the number of comparators by folding the input signal [24] into smaller repeating ranges much like modulo arithmetic or clock arithmetic [25]. This helps in reducing the device count, area and power dissipation. The system comprises of a 2-Bit Fine ADC followed by a folding block (Fig. 6) and a 2-Bit Coarse ADC, running in parallel as shown in Fig. 6. The two Least Significant Bits (LSB) are generated by the Fine ADC while the two Most Significant Bits (MSB) by the Coarse ADC, giving together a 4-Bit output. In this way only six comparators are required instead of fifteen for a 4-bit analogue to digital conversion. As a result, the simulated power dissipation of a complete ADC is reduced by approximately 58% (~140mW). This method generates the output in Gray Code instead of Binary Code which is an additional benefit. Gray Code has better immunity against meta-stability errors because only one bit changes at a time. However, folding a signal is at the expense of a higher sampling frequency.

CONCLUSIONS

The continuing research into the design an ultra low-power 4-Bit A/D converter for use in the upcoming Square Kilometre Array (SKA) is presented in this paper. The ADC operates at 4GHz sampling frequency with an analogue input bandwidth from DC to Nyquist frequency. The main engineering challenge is to design the ADC to operate at ~100mW and cost little to manufacture. To meet these targets, in-expensive optical lithographic techniques are required, in addition to designs that minimise both power dissipation and chip area. One design currently under investigation is the flash folding ADC, which has demonstrated a power consumption of ~140mW. With further optimisation of the transistor epilayer design, an ultra-low power, GHz class ADC is possible using this technology. A prototype MMIC circuit using the above design is presently being built.

ACKNOWLEDGEMENT

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List of Figures

List of Tables

Figure 1 Measured and Simulated Common-emitter I-V Characteristi

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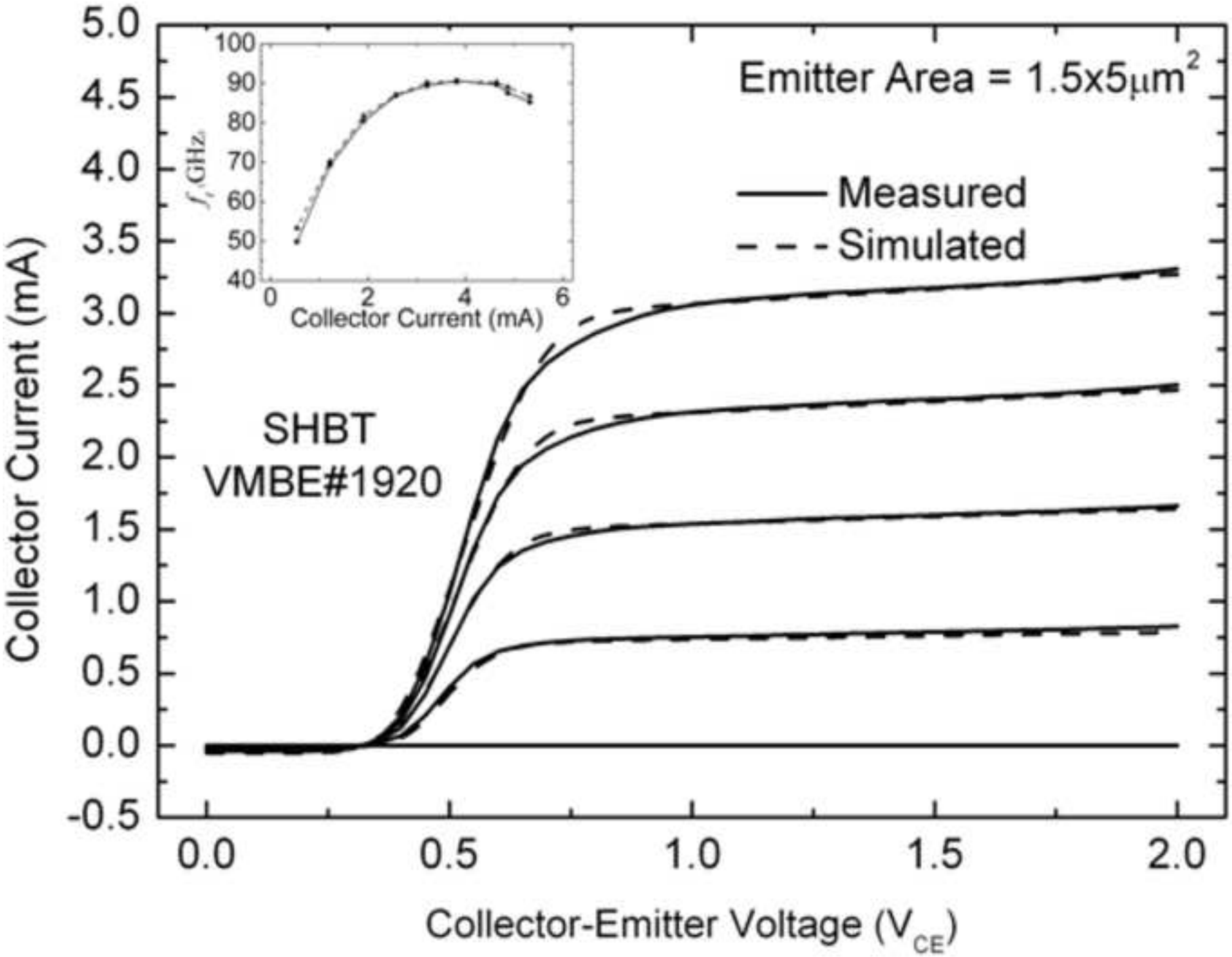

Figure 2 Schematic of Comparator cell

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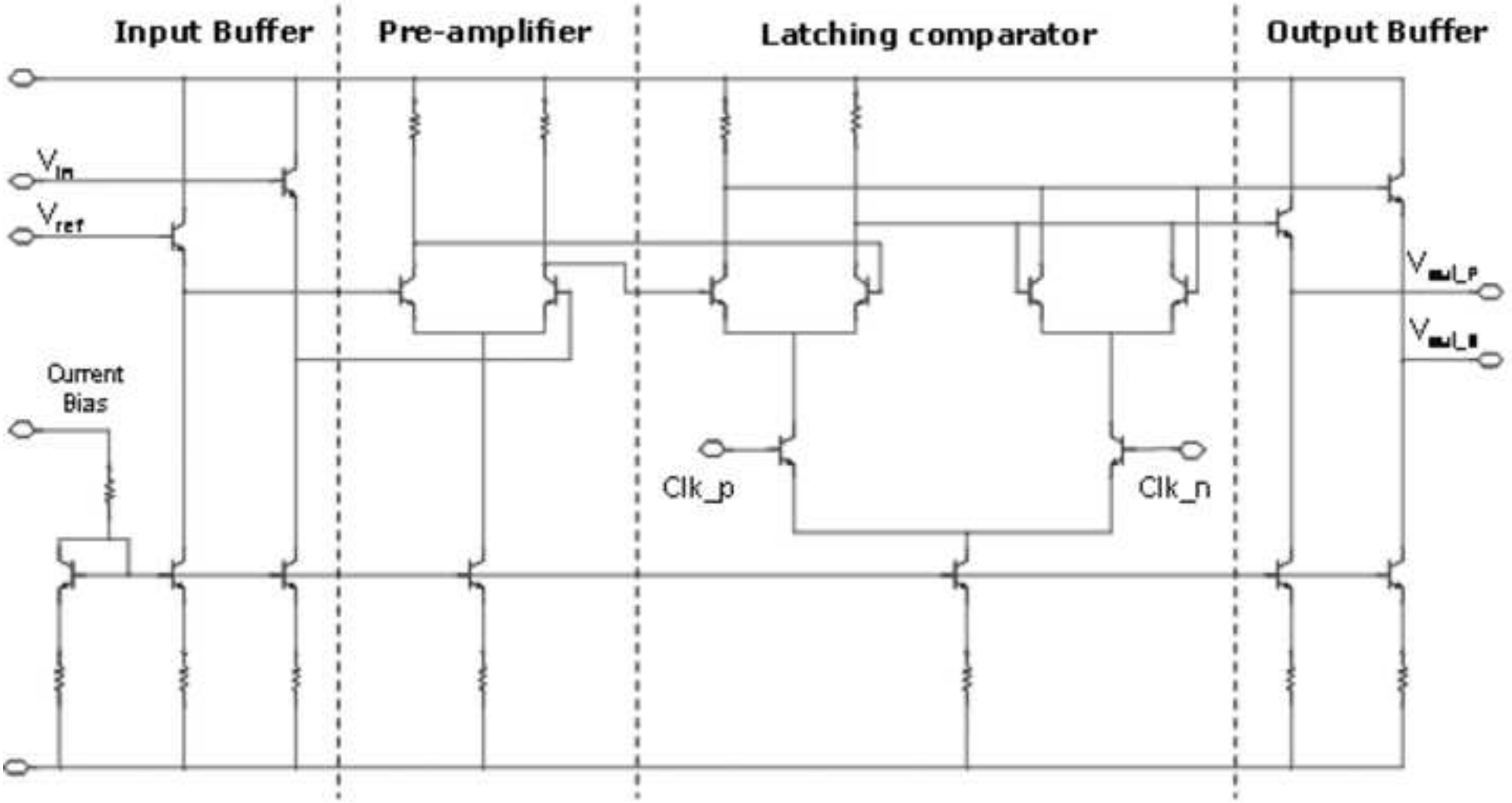

Figure 3 Recovery Time Verses Tail Current of Latched Comparator
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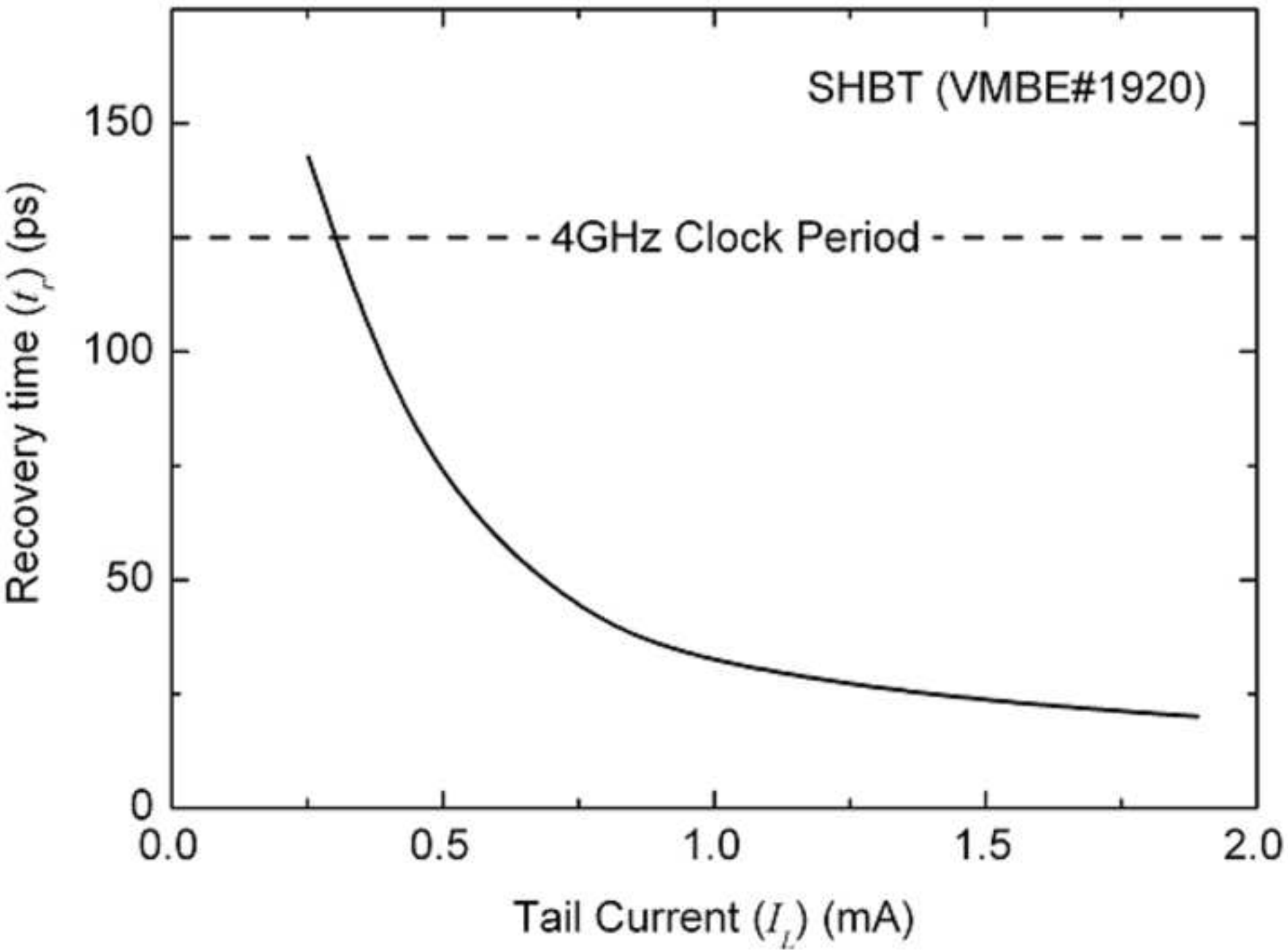

Figure 4 Comparator Output Simulated with a 4GHz clock and 1-Ghz
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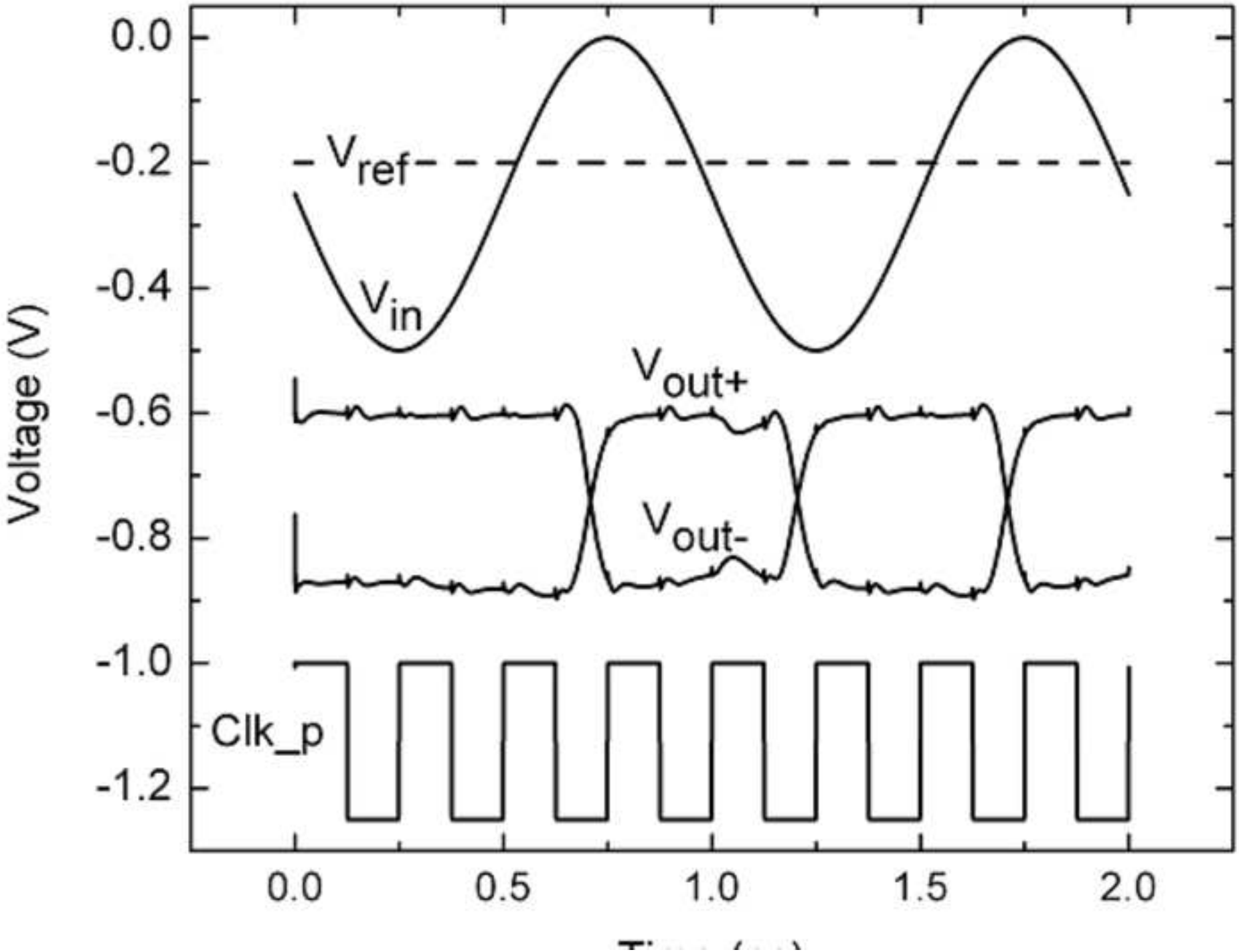

Figure 5 Common-Emitter I-V Characteristics Curves Comparison

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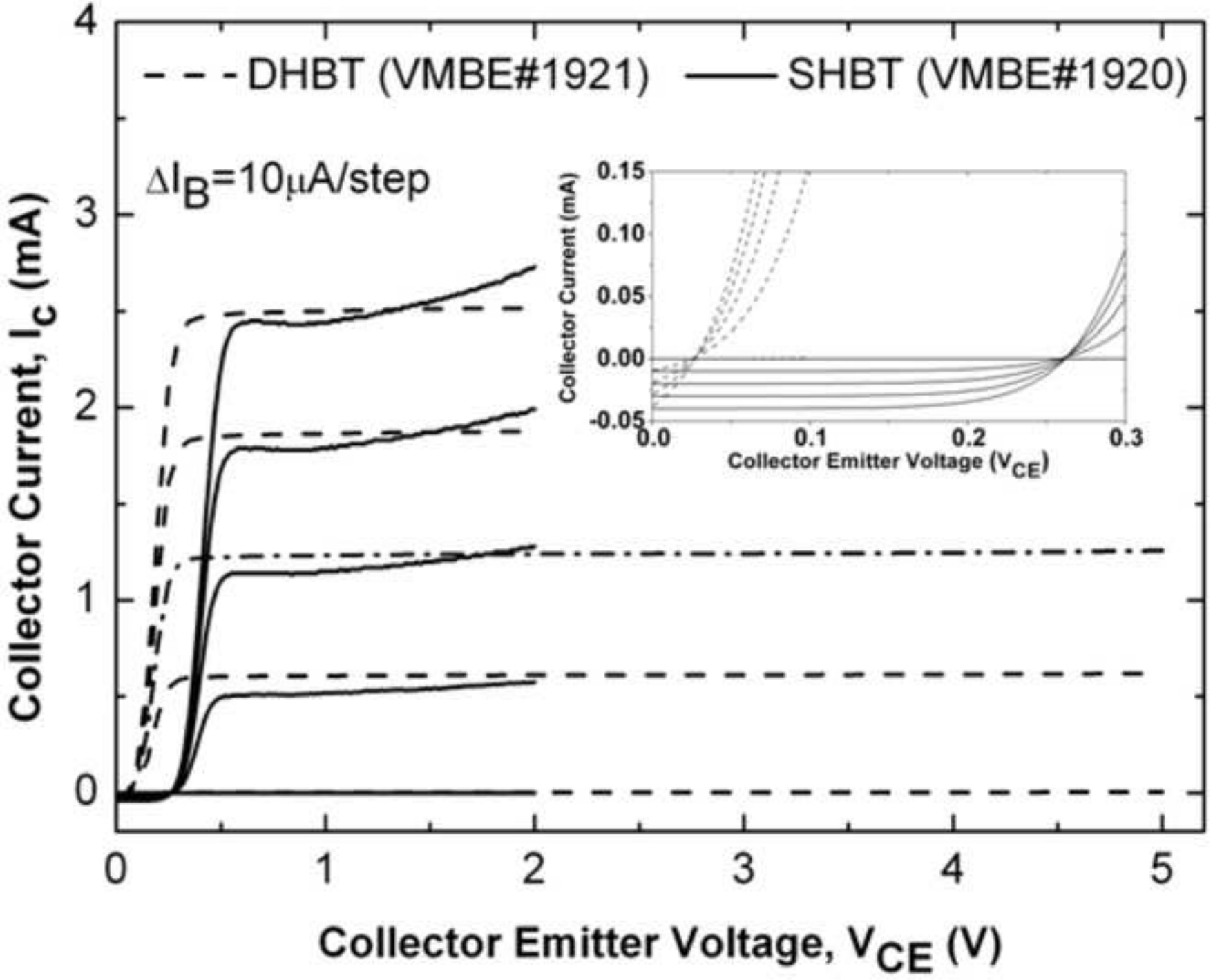

Figure 6 Folding Amplifier Schematics

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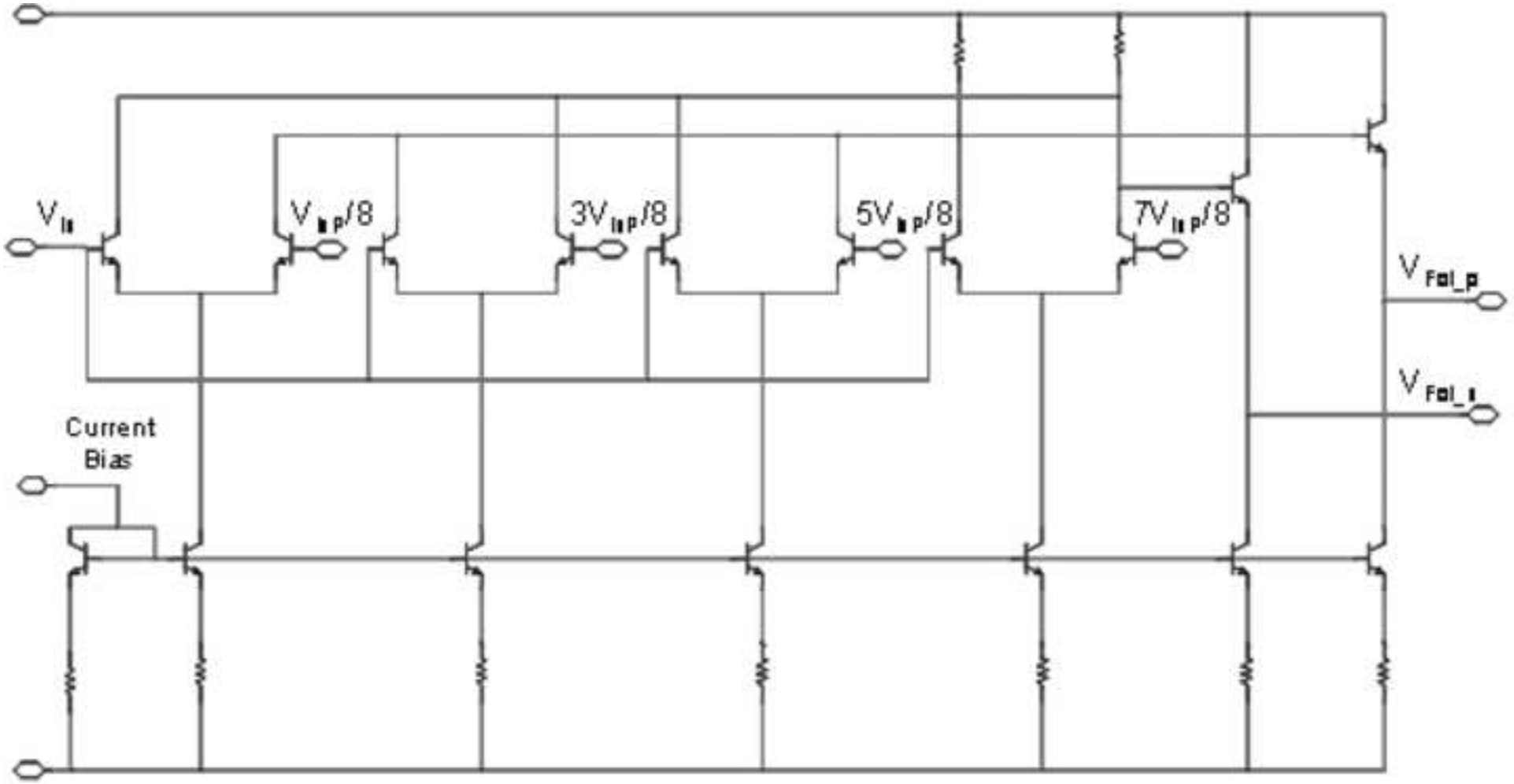

Table 1 Epitaxial Structure of SHBT and DHBT

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Layer	Composition	Thickness (Å)		Doping (cm^{-3})	
		SHBT	DHBT	SHBT	DHBT
Cap	n^{++} InGaAs	1350	1500	1×10^{19}	1×10^{19}
Emitter 1	n^{-} InGaAs	1350	1500	5×10^{17}	5×10^{17}
Emitter 2	N^{-}InP	400	400	5×10^{17}	5×10^{17}
Spacer	i-InGaAs	50	50	-	-
Base	p^{++} InGaAs	650	650	2.5×10^{19}	2.5×10^{19}
Collector	n^{-} InGaAs	6300	500	1×10^{16}	1×10^{16}
	p^{+} InGaAs	-	100	-	1×10^{18}
	N^{+} InP	-	100	-	1×10^{18}
	N^{-} InP	-	2000	-	1×10^{16}
Sub-collector	n^{++} InGaAs	5000	5000	1×10^{19}	1×10^{19}
Buffer	i-InGaAs	100	100	-	-
Semi-Insulating InP substrate					