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Modelling and simulation of low-frequency broadband LNA using InGaAs/InAlAs structures: A new approach

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ABSTRACT

The ultra-low leakage properties of a novel InGaAs/InAlAs/InP structure have been used to fabricate large gate periphery pHEMTs (up to 1200 μm^2) required for wide band low-noise amplifiers (LNA). The devices were characterized and both linear and non-linear models were extracted. LNAs were then designed and compared favourably with the best results reported to date between 0.3 and 2 GHz, still using a 1 μm gate length optical lithography.

1. Introduction

With the Si CMOS industry trends towards scaling below the 22 nm node, the issue of gate leakage is becoming ever more prominent [1,2]. While integration in CMOS-like technologies would indeed be a great benefit for low-noise amplifier (LNA) integration, superior material properties are still needed to achieve this. The most promising material system for millimetre-wave low-noise applications, however, is the InGaAs/InAlAs on InP [3,4]. The large conduction-band discontinuity ΔEc, between highly strained $In_{0.7}Ga_{0.3}As$ and $In_{0.52}Al_{0.48}As$, lattice-matched to InP, provides carrier confinement, while the high doping efficiency of Si in AlInAs results in a large sheet charge density. This, along with the high electron mobility μ in $In_{0.7}Ga_{0.3}As$ at 300 K (13,000 $cm^{-2}V^{-1}s^{-1}$), results in an extremely low resistivity of the two-dimensional electron gas (2-DEG) and impressive output characteristics [5–9]. We report here the application of such a new epitaxial layer design permitting extremely low leakage current and hence the design and fabrication of very large active devices. These studies are motivated by the design of the new generation radio telescope, the Square-Kilometre Array (SKA) telescope, which has pointed out the difficulty in making ultra LNAs operating at very low frequencies (between 0.3 and 2 GHz). The main problem resides in keeping low-noise amplification over a wide frequency band at such low frequencies. In order to achieve low NF_{min} and NF for the LNA across the frequency band, the noise resistance Rn must be substantially decreased to make the system insensitive to impedance matching. This can only be realized through the fabrication of very large gate width InGaAs/InAlAs pHEMTs, which have been successfully fabricated, measured and modelled in both linear and non-linear models. In this paper, we present the results on the measurement and modelling of active devices with very low leakage current even in structure as large as $1 \times 1200\,\mu m^2$, together with LNA simulations. We also show that InGaAs/InAlAs pHEMT on InP is a strong contender for

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ultra-low-noise applications in C-band, even when using a 1 μm gate length optical lithography process.

2. Experimental details

The epitaxial structure used in this study (wafer XMBE109) was grown using a solid-source V100 MBE system (Oxford Instruments VG Semicon). It consisted of an InAlAs buffer, strained $In_{0.7}Ga_{0.3}As$ channel, δ-doped $In_{0.52}Al_{0.48}As$ supply and undoped $In_{0.53}Ga_{0.47}As$ cap layer, as shown in Fig. 1. Mobilities as high as $\sim$13,000 cm^{-2} V^{-1} s^{-1} have been obtained by Hall measurements at room temperature. The low leakage properties of the material are attributed to both the exact level of sheet carriers in the 2-DEG and the careful control of the spacer thickness (details growth parameters are given elsewhere [10]). The high mobility together with the low resistivity of the channel improves NF_{min} via the increase of the cut-off frequency F_t and the reduction of the source resistance R_s. In addition, the noise resistance R_n is also decreased due to the higher transconductance G_m obtained by using large gate periphery devices.

Source and drain Ohmic contact formation were subsequently formed by thermal evaporation and lift-off of AuGe/Au alloyed at 320 °C, in N_2 environment. The gate electrode was then deposited by thermal evaporation and lift-off of Ti/Au. Next, Ti/Au probe pads were deposited and sintered at 300 °C to improve the Schottky contact. The devices fabricated on this wafer had identical planar structures with a gate length of 1 μm and widths ranging from 200 to 1200 μm using 2, 4 and 6 gate fingers. DC and RF characteristics of the devices were measured using a standard *S*-parameter on-wafer measurement system consisting of an Agilent 85107C system, HP 4142B DC supply and Cascade RF probes using IC-Cap. The VNA calibration was performed following the LRRM method [11] using WinCal XE and led to ±0.03 dB error.

3. Results and discussion

3.1. Large gate periphery devices

The transistors have been designed in order to make ultra-wide band LNAs operating at frequencies from 0.3 to 2 GHz. Therefore, the active devices used, here InGaAs/InAlAs/InP pHEMTs, will have to exhibit both a very low minimum noise figure NF_{min} and very-low-noise resistance R_n in order to match the input impedance from the antenna across the whole frequency band in a 50 Ω system. The noise figure of a two-port network can be expressed as follows:

$$NF = NF_{min} + \frac{4R_n}{Z_0}\frac{|\Gamma_S - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_S|^2)} \quad (1)$$

where the four noise parameters are defined as follows:

- Γ_S and Γ_{opt} are the source and optimum reflection coefficients, respectively,
- NF_{min} is the minimum noise factor expected when $\Gamma_S = \Gamma_{opt}$,
- R_n is the noise resistance,
- G_{opt} and B_{opt} are the real and imaginary parts of the optimal source admittance Y_{opt} for which:

$$\Gamma_{opt} = \frac{1 - Z_0 Y_{opt}}{1 + Z_0 Y_{opt}} \quad (2)$$

- Z_0 is the system impedance (here 50 Ω).

The important role of the noise resistance R_n of the transistor is obvious from Eq. (1). A high R_n leads to increased mismatch between the device noise figure NF and minimum noise figure NF_{min} and in addition, it also makes the design of MMIC LNAs more difficult as it usually results in poor input and output reflection coefficients. However, large gate peripheries are required in order to reduce the noise resistance [12].

In order to achieve this, large gate periphery transistors, with gate peripheries up to 1200 μm^2 have been fabricated. This was permitted by the very low leakage and high breakdown properties of the epitaxial layers as reported earlier [13]. Fig. 2 shows the gate leakage current of two large devices, 800 and 1200 μm^2, at different drain voltages. The overall level of on-state leakage is about 60

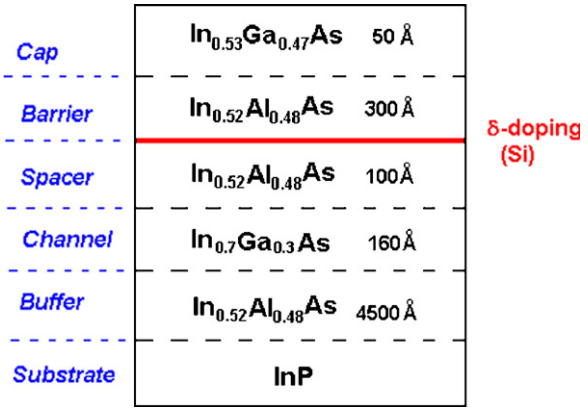

Fig. 1. Epitaxial structure of the InGaAs/InAlAs pHEMT.

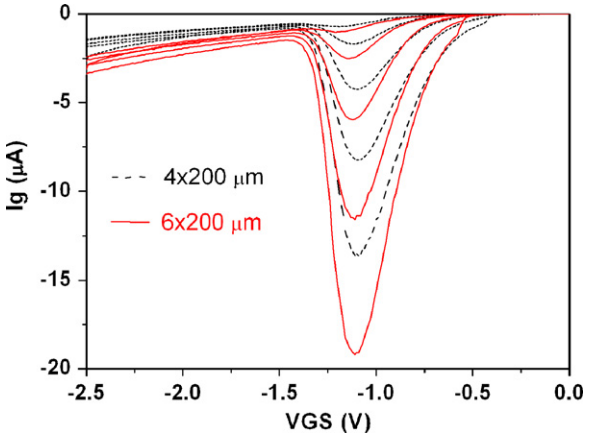

Fig. 2. Typical InGaAs/InAlAs pHEMT experimental gate current curves for two large gate periphery transistors as a function of the drain and gate voltages. VDS varies from 1 to 2 V from top to bottom in increments of −0.25 V.

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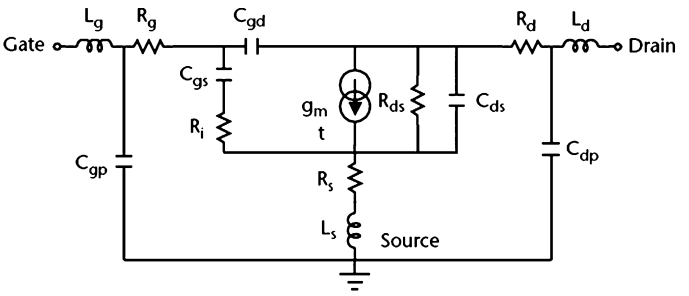

Fig. 3. Small-signal equivalent circuit of a field effect transistor.

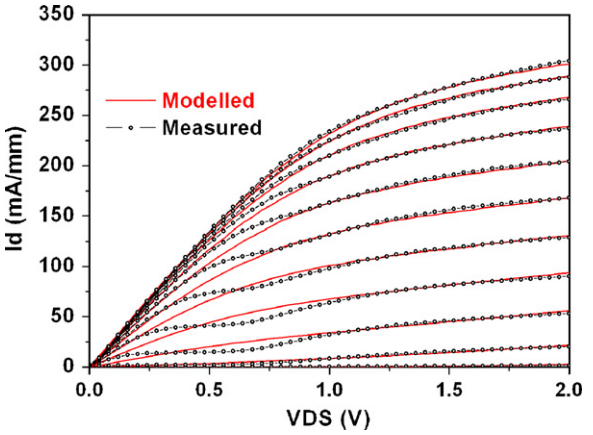

Fig. 4. Normalised measured and modelled DC characteristics of a fabricated InGaAs/InAlAs pHEMTS. VGS varies from 0 to −1.3 V from top to bottom.

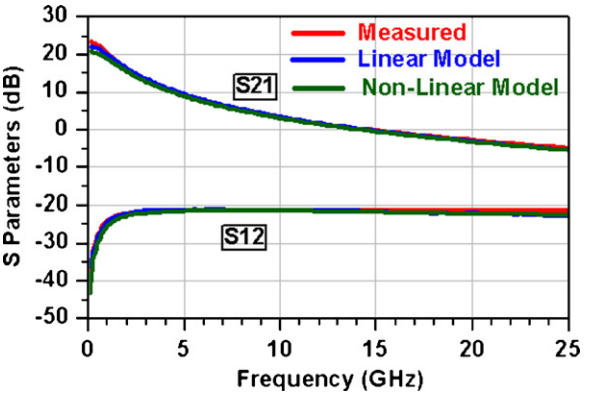

Fig. 5. Measured and simulated $S(x, y)$ as a function of frequency.

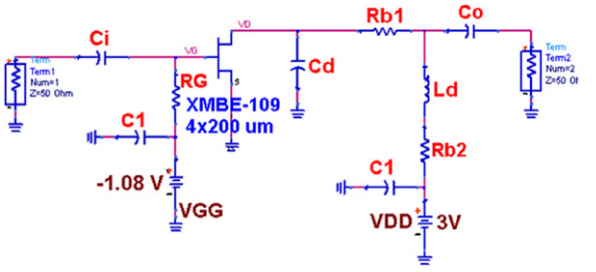

Fig. 6. LNA circuit simulation using a modelled $1 \times 800\,\mu m^2$ transistor (design 1). The transistor is biased at about 10% IDSS and all components are on-chip (full MMIC).

times lower than a typical 0.15 μm × 40 μm gate InP-based HEMT [14]. This is emphasized by the shape of the leakage curve, which clearly shows a very low level of tunnelling for higher gate-source voltage. This also shows that the on-state gate leakage is mainly due to impact ionization as a result of the hole current. In addition, these devices showed a very high breakdown voltage in excess of −15 V.

3.2. Linear and non-linear modelling

The linear small-signal model parameters were extracted from the measured *S*-parameter using standard Computer-Aided Design (CAD) tools. The 7 intrinsic model parameters were obtained from hot (active) device bias points, while the 8 extrinsic (parasitic) elements were obtained from cold (pinched) device measurements [15]. Fig. 3 shows the equivalent circuit used for the linear model. The final element values for this model were determined by applying CAD optimisation techniques to the initial values obtained, until the model accurately fitted the measured data.

The non-linear modelling was performed using the Agilent EE-HEMT model available in IC-Cap. The measurements were first performed with IC-Cap and then optimised until the model fitted the measured data. More details about the precise parameter extraction method can be found in [16]. The model was first optimised in order to fit the measured DC data. Fig. 4 shows the modelled and measured DC characteristics of a fabricated $4 \times 200\,\mu m$ pHEMT. It shows a good DC fit between the non-linear model and measured data. However, the fact that the kink effect was not taken into account in the model led to small discrepancies at low VDS. This is being investigated and will be discussed at a later stage.

The model was then optimised in order to fit the RF measured data. Fig. 5 shows the measured and modelled $S(x, y)$ for frequencies up to 25 GHz. Both the linear and non-linear models show excellent agreement with the measured *S*-parameters. Similarly, the modelled $S(x, x)$ also fit reasonably well the measured data (not shown here). The non-linear model permitted R_n to be extracted.

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Table 1
Summary of simulated LNAs using the modelled $1 \times 800\,\mu m^2$ transistors

	Stability	Gain (dB) at 1.4 GHz	S11 (dB) at 1.4 GHz	S22 (dB) at 1.4 GHz	NFmin (dB) at 1.4 GHz	NF (dB) at 1.4 GHz	NF (dB) at 2 GHz	Pdiss (mw)
1. Single-stage	OK	11.90	−2.3	−17	0.52	0.74	0.95	~60
2. Single-stage off	OK	10.45	−6.3	−21	0.53	0.61	>1	~55
3. Double-stage off	OK	26	−8.4	−14.8	0.28	0.34	0.45	~110

For the device used in the LNA simulations ($4 \times 200\,\mu m$), the noise resistance under optimal noise conditions was about 5 Ω where NF_{min} was about 0.5 dB at 2 GHz. From DC and RF measurements, the cut-off frequency F_t and maximum oscillation frequency F_{max} were 30 and 35 GHz, respectively. The output transconductance G_m was 300 mS/mm whereas the pinch-off voltage V_p was −1.3 V.

3.3. LNA designs

Comparing the characterization and modelling results from the pHEMTs of different gate peripheries, the $4 \times 200\,\mu m$ devices have been selected for LNA designs. This is mainly due the reasonably low NF_{min} (~0.5 dB at 2 GHz) and very low R_n (~5 Ω) achieved by these devices, hence minimising matching network size and losses.

Three LNA designs are presented in this paper: design 1 is single-stage MMIC, design 2 is single-stage with some off-chip components, and design 3 is double-stage with off-chip components as well. Fig. 6 shows the schematic circuit of the LNA simulated (design 1) using the $1 \times 800\,\mu m^2$ transistor biased at 10% IDSS. Since monolithic inductors generate substantial losses due to the series resistance that directly adds into the gate, no inductor was used at the input. The overall noise figure NF was below 1 dB across the whole frequency band with gain of about 12 dB at 1.4 GHz.

Similarly, LNA design 2 was done a single-stage configuration using the same active device, but had off-chip components. This design offered a new degree of freedom as an inductor could be used in the input for better matching. Table 1 shows a summary of the 3 LNA characteristics. The main improvement compared with design 1 was the input reflection coefficient S11 that was decreased from −2.3 to −6.3 at 1.4 GHz. This is an important characteristic as S11 close to zero will result in power being mainly reflected to the source and will possibly generate oscillations.

Design 3 was double-stage, and similarly to design 1, it comprised some input off-chip components. Clear improvements were observed as NF dropped to ~0.35 dB at 1.4 GHz. The gain was also increased to about 26 dB, while the input reflection coefficient was decreased as the expense of the power dissipation that doubled. The LNA simulations also showed high linearity as evidenced by the third-order intercept IP3 of −14 dBm. These results are amongst the best reported to date at this frequency band compare favourably with those reported in the literature but using much smaller gate lengths, 0.90 μm Si CMOS [17], 0.15 μm InGaAs/InAlAs [18] or 0.5 μm GaAs pHEMTs [19]. The use of this material structure is currently being investigating at sub-micron gate lengths but still using optical lithography.

4. Conclusions

Large gate periphery pHEMTs have been fabricated on novel InGaAs/InAlAs/InP structure especially designed to limit current leakage and to exhibit high breakdown voltage. The transistors have been measured and showed excellent agreement with both linear and non-linear models. LNAs operating form 0.3 to 2 GHz have been designed using these active devices and have shown excellent characteristics for low noise, impedance matching and linearity. The ultra-low level of leakage exhibited by this material structure has shown to be promising for post Si CMOS era.

Acknowledgements

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References

[1] Yu B, Wang H, Riccobene C, Xiang Q, Lin M-R. In: IEEE symposium on VLSI technology digest of technical papers, 2000. p. 90.
[2] Guindi RS, Najm FN. In: IEEE Proceedings of the fourth international symposium on quality electronic design (ISQED'03), 2003.
[3] Pospieszalski MW. IEEE Microwave Magazine, Septembre 2005, p. 62–75.
[4] Pospieszalski MW, Wollack EJ. In: Proceedings of gallium arsenide applications symposium (GAAS), 2000.
[5] Mishra UK, Brown AS, Rosenbaum SE, Hooper CE, Pierce MW, Delaney MJ, et al. IEEE Electron Device Lett 1988;9(12):647.
[6] Mishra UK, Brown AS, Jelolian LM, Hackett LH, Delaney MJ. IEEE Electron Device Lett 1988;9(1):41.
[7] Matloubian M, Jelloian LM, Lui M, Liu T, Thompson MA. IEEE Electron Device Meet IEDM Digest 1993:915–7.
[8] Suemitsu T, Tokumitsu M. IEICE Trans Electron 2007;E90–C(5).
[9] Kim D-H, Del Alamo JA, Lee J-H, Seo K-S. IPRM 2007, p. 51.
[10] Missous, M. Patent pending.
[11] Davidson A, Jones K, Strid E. ARFTG conference digest—Fall, 36th, vol. 8, 1990, p. 57–63.
[12] Fukui H. Bell Syst Tech J 1979;58:771–97.
[13] Bouloukou A, Sobih A, Kettle D, Sly J, Missous M. In: Proceedings of the seventh MINT millimeter-wave international symposium—MINT-MIS, 2006.
[14] Webster RT, Wu S, Anwar AFM. IEEE Electron Device Lett 2000;21:193–5.
[15] Berroth M, Bosch R. IEEE Trans Microwave Theory Tech 1990;38(7):891–5.
[16] Agilent Technologies, IC-CAP nonlinear device models. Agilent Technologies, May 2004.
[17] Belostotski L, Haslett JW. In: IEEE radio and wireless symposium, Long Beach, 2007, p. 221–4.
[18] Rosenbaum SE, Jelloian LM, Larson LE, Mishra UK, Pierson DA, Thompson MS, et al. IEEE Microwave Guided Wave Lett 1993;3(8):265–7.
[19] Xu J, Woestenburg B, Geralt bij de Vaate J, Serdijn WA. Electr Lett 2005;41.

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