A Differential SiP (LNA-filter-mixer) in Silicon Technology for the SKA Project

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***Abstract*— This paper describes two filters realised in a technology entirely dedicated to passive components and which allows active dies flip-chip by means of bumps. Then, it presents the design of a SiP (System in Package) constituted of a differential LNA (Low Noise Amplifier) and mixer flipped respectively in front and back of a balanced filter. Measurements of a SiP, where just the LNA is flipped onto the filter, are shown in the last part.**

I. Introduction

Several projects of large radiotelescopes as LOFAR (Low Frequency Array) and SKA (Square Kilometer Array) are currently under development. They will be made up of thousands of antennae and so of thousands of front-end receivers. Each receiver includes a LNA, a filter and a mixer. The scope is then to reach the maximum integration scale to simplify the inter-circuits connections and reduce losses from the lines.

In the first two parts, this paper presents a passive technology used as inter-connection substrate between active dies, but also as a passive technology, which allows the design of wide band-pass filter. Section IV deals with the flip-chip technique and the design of a SiP where two actives dies (a differential LNA and a differential mixer) are respectively flipped in front and back of a passive balanced filter. Finally, measurements of the SiP, where only the LNA is flipped onto the filter, are presented.

II. The PICS technology

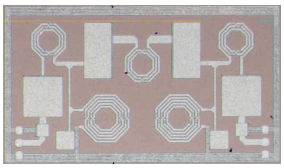
The PICS technology (Passive Integration Connecting Substrate) proposed by NXP Semiconductors, is based on a highly resistive silicon substrate. Above it, several layers are used to realise 3D and planar capacitors. Their respective typical capacitor density is 25nF/mm² and 1,2nF/mm². The next layer is polysilicon. On the top, there are two metallisation layers in aluminium. MIM capacitors of 80pF/mm² typical density and symmetrical inductors are designed in these layers. Finally, this technology offers two bumps inter-connections levels. The first one is for the attachment of an active die to the PICS and the second one refers to the assembly of the SiP into a package. The second interconnect can also be done for wire-bonding.

III. Realisation of two band-pass filters

The low operating frequency band of SKA is between 0.1 and 1.4 GHz. But in this study, we work between 0.35 and 2 GHz. This corresponds to the -3dB passband of the desired filter. The other specifications are no ripple in the band, a high selectivity, 60dB of rejection and a 50 ohms matching. The topology chosen for the filters is a classical Tchebychev structure. Two filters have been realised. The first one is a single-ended and the second one uses the same structure in a balanced configuration.

A. Single-ended band pass filter

To maintain a good trade-off between selectivity and losses, a 5th-order filter has been chosen. To increase the selectivity at high frequencies, 2nd-order low-pass filters have been added at each side of the Tchebychev structure. The photograph of the filter is shown in Fig. 1.



(2.8´1.6 mm²)

Fig. 1 Photograph of the single-ended 5th-order Tchebychev band pass filter

Schematic, electrical simulations and layout are done with Cadence software. As the filter is composed of resonant elements and quite long inter-connection lines, electromagnetical (EM) simulations performed with the ADS Momentum software are necessary to adjust the value and disposition of the components.

Probe station measurements and Momentum simulations are presented in Fig. 2.

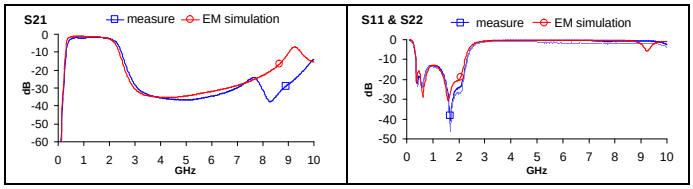
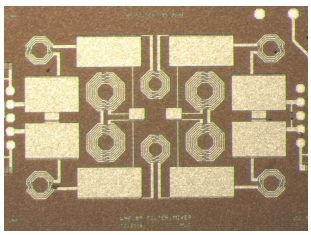


Fig. 2 Measurements and EM simulations of the single-ended filter

A quite good agreement is obtained between EM simulations and measurements, with a good matching in the passband. However, the rejection does not reach the 60dB goal. Post simulations of the schematic, including the equivalent inductors of lines to the ground, have shown that the length of the lines between capacitors and ground are very sensitive and have a large effect on the out-of-band rejection.

B. Balanced band pass filter

The previous filter is now transformed into a balanced structure because SKA antennae should be dipoles. Consequently, a part of the front-end receiver can be in a differential configuration. Components in the transmission line of the filter are the same, and those in shunt are multiplied by 2 for the inductors and divided by 2 for the capacitors. The photograph of this balanced filter is shown in Fig. 3.



(2.7´1.5 mm²)

Fig. 3 Photograph of the balanced 5th order Tchebychev band pass filter

To save space, lines width of the inductors and the space between turns have been decreased compared to the single-ended filter. Moreover, instead of using a single large inductor, two smaller inductors are used in series. Thus, the balanced filter has almost the same dimensions as the single-ended version.

Fig. 4 presents the on-chip measurements with the EM simulations. Usually, differential circuits are measured by mean of baluns. But this approach generates inaccuracies and does not give access to all the parameters as the conversion from common mode to differential mode for example. However, Bockelman et al. addressed the issue by adapting single-ended S-parameters for use with differential circuits [1]. These S-parameters are called mixed-mode S-parameters, and characterise the differential mode (Sdd_{ij}), the common mode (Scc_{ij}), the conversion from differential to common mode (Scd_{ij}) and the conversion from common to differential mode (Sdc_{ij}) (i & j = 1 or 2). A 4-port is then characterised by 16 mixed-mode S-parameters, which are each expressed as a function of the 2-port S-parameters [2]. Consequently, we have used GSGSG probes and a 4-port E5071B VNA (Vector Network Analyser) from Agilent Technologies for these balanced measurements.

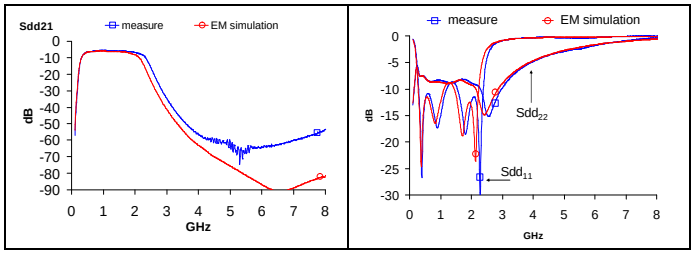


Fig. 4 Measurements and EM simulations of the balanced filter

The pass band of the filter is a little wider than expected by the simulation, but there is a quite good agreement between measurements and EM simulations. The 5dB losses and poor Sdd_{22} are due to a 100-ohm resistor placed between the two output ports. This resistor is used for the input matching of the mixer. In this case, the rejection reaches the 60dB goal and is much better than the single-ended filter. Therefore, the lines to the ground in the single-ended filter limit the rejection of the response. Fig. 5 shows the measurements results of the single-ended filter and the balanced filter.

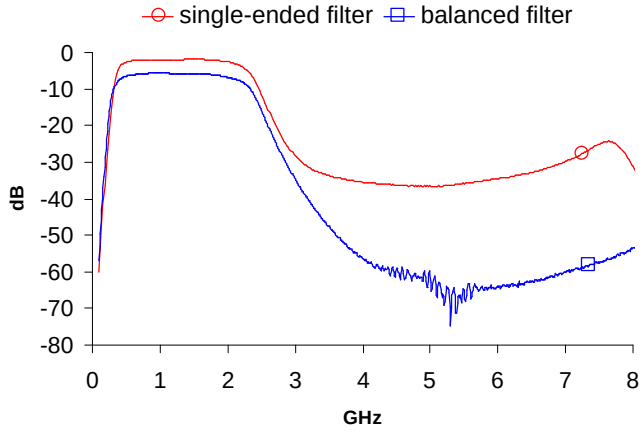


Fig. 5 Measurements of the two filters

IV. SiP Design and Measurements

A. Flip-Chip Assembly

To realize a SiP composed of 3 basic functions: a differential SiGe LNA, a balanced PICS filter and a differential SiGe mixer, the flip-chip assembly is used. In this technique, the active dies are upside down onto a substrate to directly connect pads by means of conductive bumps. As the inter-chip connections are no more wire bonds or lines of a board, the effects induced by those are reduced and the performances improved.

The flip-chip assembly is done in 3 stages. First, the die or the wafer is bumped, then the bumped die is connected to a substrate or a board and finally, the under-chip space is usually filled with underfill. Underfill is a non-conductive

adhesive, which joins the entire surface of the active die to the substrate or board. It protects the inter-connection area from the moisture, consolidates the mechanical connections and improves the thermal dissipation. Without underfill, a difference in the coefficient of thermal expansion can indeed, break or damage the electrical connection of the bumps [3].

Several kind of flip-chip assembly, in particular kind of bumps, are existing. The most known are the solder bump, the plated bump and the stud bump [4]. Before realising these bumps, an under bump metallization (UBM) is often required because Silicon chips have aluminium (Al) pads and ordinary solders do not wet to Al. UBM is therefore placed on the chip pads to replace the insulating aluminium oxide layer and delimit the solder-wetted area. This operation can be done by sputtering, plating or chemical treatment. In solder bump process, the solder is deposited over the UBM by evaporation, electroplating, screen printing solder paste or needle-depositing. Then the bumped die is flipped onto the substrate and the assembly is heated to do solder connection. In plated bump, the aluminium oxide is first removed by wet chemical process and conductive metal bumps are then plated on the pads. Bumps are in nickel-gold and are formed by electroless nickel plating of the Al pads. A gold layer is added for protection. And the stud bump process is a modified version of the standard wire bonding process. To form the stud bump, gold wire bonds are attached to the pads of the die and then melting at their end to obtain a ball [5].

As we just need few examples of the SiP, gold stud bump process has been used. Bumps of NXP Semiconductors measure 30µm height and 50µm of diameter. Their electrical models are equivalent to a resistance in serial with an inductor of respectively 60mΩ and 28pH, which is negligible. Flip-chip assembly is represented in Fig. 6.

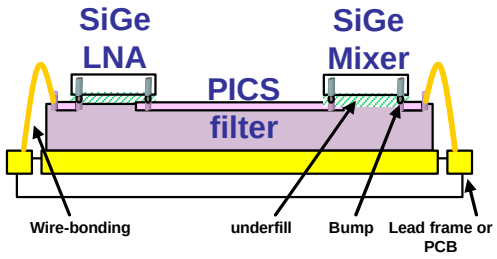


Fig. 6 Cross-section of the SiP

B. SiP Design

As explained previously, the PICS technology does not only allow to design passive filters but allows actives dies flip-chip too. Therefore, to realise a SiP, a new layout has been designed in PICS technology. This layout is composed of the balanced band pass filter seen in section III, in front of it the footprints of the differential LNA and back of it, the footprints of the differential mixer. As the PICS technology offers high density capacitors, several have been put on the power supplies of the active dies to realise decoupling capacitors of 20pF, 150pF and 5nF. Test pads have been inserted for probe measurements of the LNA flipped onto the filter and bigger pads have been added to wire-bond the complete SiP to an external board. A photograph of it without the actives dies are shown in Fig. 7.

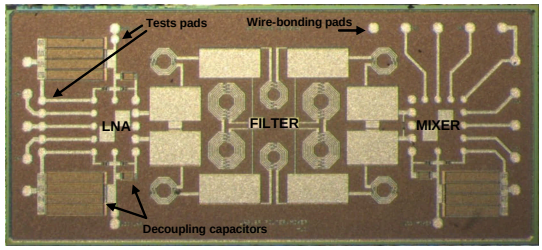


Fig. 7 Photograph of PICS substrate (5.2×2.3mm)

C. SiP Measurements

For the measurement of the SiP, we proceed in several steps. First, the on-chip measurements of the filter alone (seen in Section III) are performed. Then, on-chip measurements of the LNA flipped onto the PICS, and finally measurements of the SiP with the LNA and mixer by mean of a test board are processed.

At now, just the probe station measurements of the SiP where the LNA is flipped onto the PICS have been performed. As for the filter alone, GSGSG probes and 4-port VNA have been used to measure the mixed-mode S-parameters. Measurements have been performed at XLIM laboratory (Limoges, France). Photograph of the SiP under test and its measurements results are shown in Fig. 8.

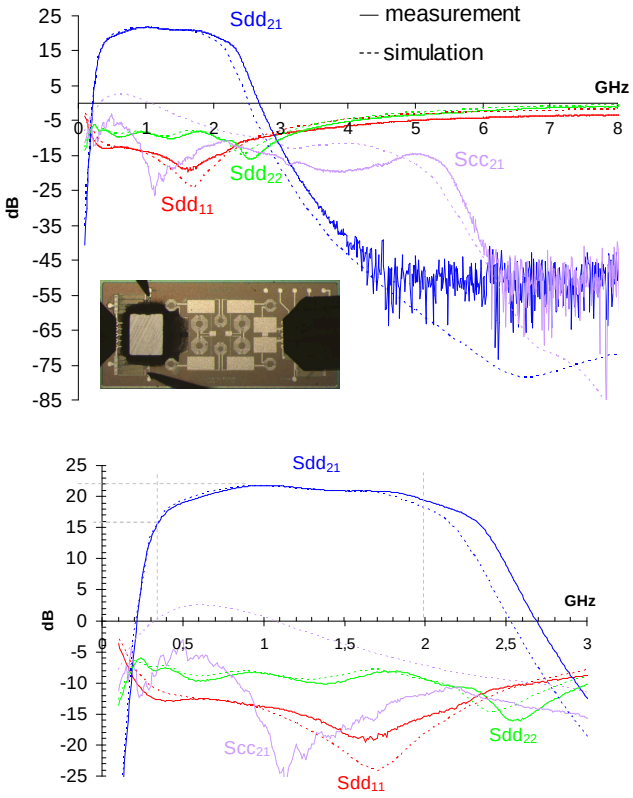


Fig. 8 Photograph of the SiP under test and its measurements results

In these graphs, results correspond to the schematic simulation of the LNA with the Momentum simulations of the filter. A quite good agreement is obtained between simulations and measurements. The gain in the pass band is quite flat with a value of about 20dB. There is a good input matching. The CMRR (Common Mode Rejection Ratio) is at least 25dB and there are no significant mode conversions. These results show that bumps have no effect on the performances of the differential LNA.

V. Conclusions

We have designed and measured a SiP (LNA-filter) with good agreement between simulations and measurements.

These first measurements demonstrate the possibility to build filters with quite high out-of-band rejection and the viability of such SiP for radioastronomical projects like SKA.

Acknowledgment

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References

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