Sub-0.5 dB NF broadband low-noise amplifier using a novel InGaAs/InAlAs/InP pHEMT

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Linear and non-linear modelling of a novel ultra-low noise InGaAs/InAlAs pHEMTs have been used to design a low noise amplifier operating from 0.3 to 2 GHz. The LNA has ~ 0.4 dB NF across the whole frequency band, power gain of 26 dB at 1.4 GHz and IP3 of 14 dBm, making it a good candidate for the aperture array concept of the Square Kilometre Array (SKA) telescope, GSM, GPS, civil and military DAB.

1. Introduction

The design and fabrication of the Square Kilometre Array (SKA) telescope, a new radio telescope which will have 100 times more sensitivity than the best telescope to date, is attracting a lot of interest in the design of broadband ultra-low noise amplifiers operating at frequencies from 0.3 GHz to 2 GHz [1]. In an effort to achieve the ultra low noise level required across the wide band, different transistor technologies have been used. However for broadband operation both minimum noise figure and noise resistance play a crucial role. The noise figure of a two port network can be expressed as follows:

$$NF = NF_{\min} + \frac{4R_n}{Z_0} \frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{\left|1+\Gamma_{opt}\right|^2 \left(1-\left|\Gamma_S\right|^2\right)} \qquad (1)$$

Where the four noise parameters are defined as follows:

- Γ_S and Γ_{opt} are the source and optimum reflection coefficients, respectively,
- NF_{min} is the minimum noise factor expected when $\Gamma_S = \Gamma_{opt}$,
- R_n is the noise resistance,
- G_{opt} and B_{opt} are the real and imaginary parts of the optimal source admittance Y_{opt} for which: $$\Gamma_{opt} = \frac{1 - Z_0 Y_{opt}}{1 + Z_0 Y_{opt}} \qquad (2)$$
- Z_0 is the system impedance (here 50Ω).

The important role of the noise resistance Rn of the transistor is obvious from equation (1). A high Rn leads to increased mismatch between the device noise figure NF and minimum noise figure NFmin and in addition, it also makes the design of MMIC LNAs more difficult as it usually results in poor input and output reflection coefficients. The superior noise performance of InP-based HEMT's was demonstrated convincingly at millimeter wave frequencies using short-gate devices [2] and used in high performance LNAs [3]. However, for low frequency applications, the requirement of extremely high cut off frequencies are relaxed and larger gate lengths (~ 1 μm), as opposed to sub-μm are perfectly adequate in term of noise performance [4]. In order to further improve the noise resistance Rn, transistors with large gate periphery (up to 1200 μm^2) have been successfully fabricated and measured. This was permitted by the very low leakage and high breakdown properties of the epitaxial layers as reported earlier [5]. The most suitable device, in terms of noise figure, noise resistance and power consumption, has been used to design a broadband ultra low noise LNA in a 50Ω system.

2. Experimental

The epitaxial structure used in this study (wafer XMBE109) was grown using a solid-source V100 MBE system (Oxford Instruments VG Semicon) at the University of Manchester. It consists of an InAlAs buffer, strained $In_{0.7}Ga_{0.3}As$ channel, δ-doped InAlAs supply and undoped InGaAs cap layer. The devices fabricated on this wafer have identical planar structures with a gate length of 1 µm and widths ranging from 200 µm to 1200 µm using 2, 4 and 6 gate fingers. Both DC and RF characteristics of the devices were measured using a standard S-parameter on-wafer measurement system consisting of an Agilent 85107C system, HP 4142B DC supply and Cascade RF probes using IC-Cap.

3. pHEMT Modelling

Extensive numerical analysis using two different modelling techniques were employed to characterize the performance of fabricated InGaAs/InAlAs/InP pHEMTs, namely, the commonly used small-signal linear model and the EE-HEMT large signal nonlinear model.

3.1 Linear Modelling

The linear small-signal model parameters were extracted from the measured S-parameter using standard computer-aided design (CAD) tools. The 7 intrinsic model parameters were obtained from hot (active) device bias points, while the 8 extrinsic (parasitic) elements were obtained from cold (pinched) device measurements [6]. The final element values for this model were determined by applying CAD optimization techniques to the initial values obtained, until the model accurately fitted the measured data. The 15 model parameters were then simulated in ADS and compared to the measured data.

3.2 Non-Linear Modelling

The non-linear modelling was performed using the Agilent EE-HEMT model available in IC-Cap. The measurements were first performed with IC-Cap and then optimised until the model fitted the measured data. More details about the precise parameter extraction method can be found in [7]. The model was first optimised in order to fit the measured DC data. Figure 1 shows the modelled and measured DC characteristics of the fabricated 4 × 200 µm pHEMT. It shows a good DC fit between the non-linear model and measured data. The model was then optimized in order to fit the RF measured data. Figure 2 shows the measured and modelled S(x,y) for frequencies up to 25 GHz. Both the linear and non-linear models show excellent agreement with the measured S-parameters. Similarly, the modelled S(x,x) also fit reasonably well the measured data (not shown here). The non-linear model permitted Rn to be extracted. For the device studied (4 × 200 µm) the noise resistance under optimal noise conditions was about 5 Ω.

4. LNA Design

The LNA design was simulated in ADS using the non-linear models of the fabricated pHEMTs, as discussed in the previous section. The input matching was achieved using off-chip inductors in order to preserve the LNA noise figure from being affected by the large series resistance (about 20-30 Ω) usually found in integrated inductors. The two-stage LNA operating from a 3V power supply was designed to include the on-chip output matching network. It consists of two common source amplifiers. The first stage was designed to provide a simultaneous noise and impedance match by carefully adjusting the two off-chip inductors at the input using a 4 × 200 µm gate width pHEMT as a building block.

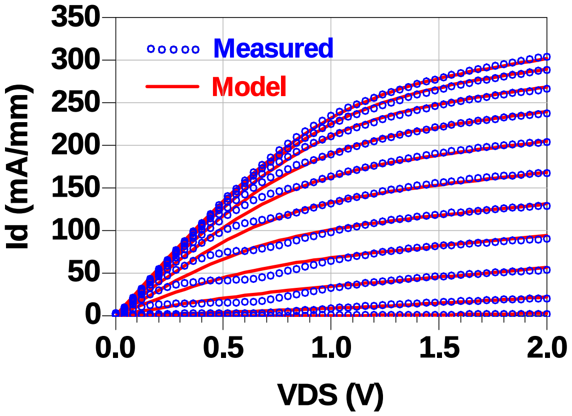

Fig. 1: Non-linear model and measured data: DC characteristics of the fabricated 4 × 200 µm InGaAs/InAlAs/InP pHEMT. From top to bottom, VGS varies 0 V to -1.3 V in increments of -0.13 V.

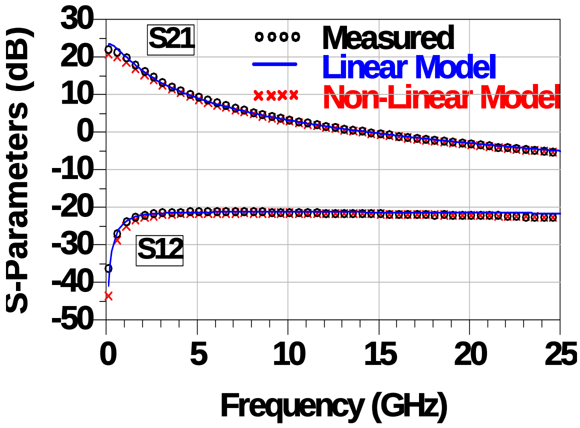

Fig. 2: Measured and modelled S-parameters for the 4 × 200 µm InGaAs/InAlAs/InP pHEMT.

The second stage also used a 4 × 200 µm pHEMT but the matching inductors were replaced by a large resistor. The transistor size was carefully chosen in order to have low Rn which can be easily achieved using this large gate periphery. The typical cut off frequency and maximum oscillation frequency of the 4 × 200 µm pHEMT were both about 35 GHz. The two transistors were biased at the same drain current Id of about 19 mA to simultaneously realise low noise figure, reasonable gain and low power dissipation.

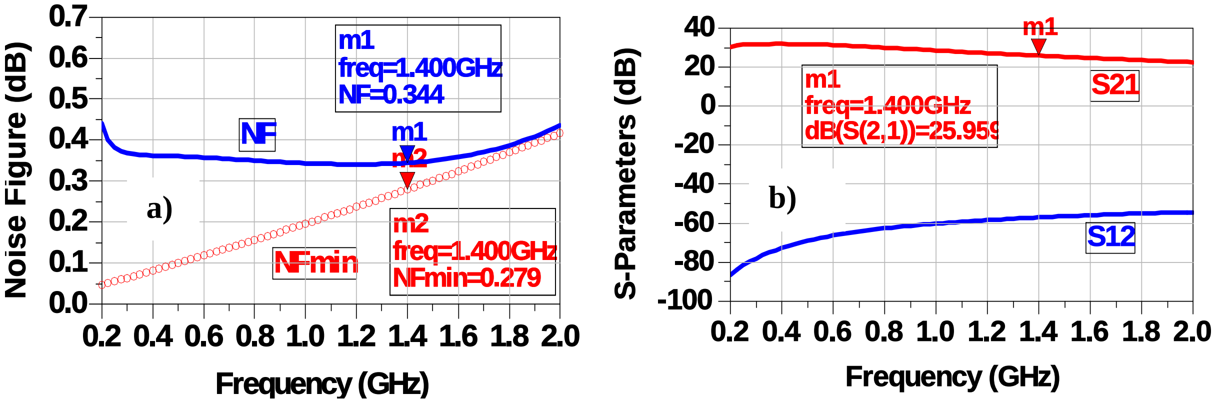

Fig. 3: LNA simulation results in a) noise figure NF and minimum noise figure and b) power gain S(21) and S(12). All parameters are expressed in dB and simulated are performed at room temperature.

Figure 3 shows the LNA simulation results. The noise figure remains below 0.45 dB between 0.3 and 2 GHz, while the gain is above 26 dB below 1.4 GHz. The input and output return losses S(11) and S(22) were below -9 dB and –14 dB, respectively at 1.4 GHz. The third order intercept obtained from LNA simulations was 14 dBm. The circuit also showed unconditional stability up to 30 GHz with a total power dissipation of 110 mW.

Table 1 shows the main simulations results compared with those reported in the literature at this frequency band. The LNA presented in this paper shows noise characteristics amongst the best published to date especially when considered in the light of the relatively large, optically defined gate length of the transistor used here (1 µm). The high gain LNA presented in [10] was obtained using a three-stage circuit which would dissipate large amounts of power but would probably have higher IP3.

Bandwidth (GHz)	0.7 – 1.4	0.6 - 1.6	2.25 – 2.5	0.3 – 2
NF (dB)	0.35	0.5	0.5	0.45
Technology	90 nm-CMOS	0.5µm GaAs pHEMT	0.15µm InGaAs-InAlAs HEMT	1 µm InGaAs-InAlAs pHEMT
Power dissipation (mW)	45	852	?	110
IP3 (dBm)	7.5	15.4	?	14
Gain (S21) dB	20.5 - 16.3	29.3 - 20.9	>35	26
Ref.	[8]	[9]	[10]	This work

Table 1: Summary of the main ultra low noise amplifiers below 2.5 GHz, at room temperature

5. Conclusions

Linear and non-linear modeling has been performed on new high breakdown, large gate periphery InP-based pHEMTs. Results show excellent agreement between measured and modeled transistor data. A double-stage wide band LNA designed with a 4 × 200 µm gate width pHEMT exhibits a noise figure below 0.45 dB from 0.3 to 2 GHz, power gain of 26 dB while dissipating a power of 110 mW. These results are believed to be amongst the best reported to date from 1 µm gate length InP-based pHEMT LNA at room temperature. The LNA design reported here is presently being fabricated.

Acknowledgements

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