Two-Dimensional Physical and Numerical Modelling of InP-based Heterojunction Bipolar Transistors

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State-of-the-art HBTs were designed, grown, fabricated and characterized in-house. The novelty of this process was the use of dimeric phosphorus generated from a Gallium Phosphide (GaP) decomposition source, which permitted growth at a fairly low temperature (420^{o}C) while conserving extremely high quality materials. A self-aligned transistor with an emitter area of 5x5μm^{2} demonstrated a low offset voltage of 150mV and high current gain of 90. An excellent agreement with the measured data was achieved using physical modelling packages developed by SILVACO.

1. Introduction

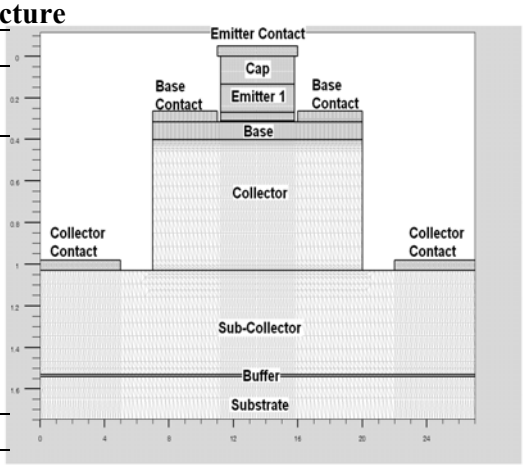
InP/InGaAs Single Heterojunction Bipolar Transistors (SHBTs) have shown excellent characteristics which make them extremely attractive for high frequency applications [1, 2]. For the next generation state-of-the-art devices, development tools are becoming increasingly necessary to fully characterise the physical phenomenon within a device. In this paper we present results of a two-dimensional DC physical modelling of InP/InGaAs HBTs using Technology-Computer-Aided-Design (TCAD) within the SILVACO software package. The effect of the spacer layer on the turn-on voltage of device is investigated in details.

2. Material Growth and Fabrication

The epitaxial layers (shown in Table 1) were grown on a VG 90H solid-source molecular beam Epitaxy (MBE) system on Fe-doped semi-insulating (100) InP substrates. Phosphorus was generated from a GaP decomposition source whose operational aspects are described elsewhere [3]. The growth was performed at a relatively low temperature of ~420^{o}C and used stoichiometric conditions for both the Arsenide and Phosphide materials.

Table I
SHBT Epilayer Structure

	InP/$In_{0.47}Ga_{0.53}As$ SHBT		
Layer	**Material**	**Doping (cm^{-3})**	**Thickness (Å)**
Cap	$In_{0.47}Ga_{0.53}As$	$n=1x10^{19}$	1350
Emitter 1	$In_{0.47}Ga_{0.53}As$	$n=1x10^{17}$	1350
Emitter 2	InP	$n=1x10^{17}$	400
Spacer	$In_{0.47}Ga_{0.53}As$	-	50
Base	$In_{0.47}Ga_{0.53}As$	$p=1.5x10^{19}$	650
Collector	$In_{0.47}Ga_{0.53}As$	$n=1x10^{16}$	6300
Sub-Collector	$In_{0.47}Ga_{0.53}As$	$n=1x10^{16}$	5000
Buffer	$In_{0.47}Ga_{0.53}As$	-	100
Substrate	Semi-Insulating InP		



3. Device Simulation

The device is carefully layered and meshed in order to improve simulation performance and avoid convergence errors in DEVEDIT, as shown in Table I. Since the current database of ATLAS does not incorporate III-V materials, an extensive research was carried out to accurately define the relevant properties of InP and InGaAs as shown in Table II. A concentration dependent Analytic mobility model which is based on the Caughey and Thomas mobility model [4] was included in the simulation to approximate the effect of doping on the mobility of electrons and holes in the material. The effective mobility of electrons and holes in a region is given Eqn.(1):

$$\mu = \mu_{\min}\left(\frac{T_L}{300}\right)^{\beta} + \frac{\mu_{\max}\left(\frac{T_L}{300}\right)^{\delta} - \mu_{\min}\left(\frac{T_L}{300}\right)^{\beta}}{1+\left(\frac{T_L}{300}\right)^{\gamma}\left(\frac{N}{N_C}\right)^{\alpha}} \quad (1)$$

where,

β, δ and γ are the temperature dependent fitting coefficients, T_L=300K. The other mobility parameters for electrons and holes of different materials are defined in Table III.

Due to the high base doping concentration, Bandgap Narrowing model is included. Recombination mechanisms are approximated by concentration dependent Schockley-Read-Hall, Auger and Band to Band recombination models. In order to simulate the break down voltage and the effect of the impact ionization, Selberherr's Model is implemented. Thermal effects are not considered in the simulations.

Table II
Material Parameters

Parameter	InP	$In_{0.47}Ga_{0.53}As$
Dielectric Permittivity	12.35[5]	13.88[5]
Energy Gap (eV)	1.35[6-8]	0.75[6-8]
Electron Affinity (eV)	4.38[7]	4.6[7]
Electron Effective Mass	0.08[6, 7]	0.041[7]
N_C (cm^{-3})	$6.4x10^{17}$[5, 6]	$8.9x10^{16}$ [5, 6]
N_V (cm^{-3})	$1x10^{19}$ [5]	$1x10^{18}$ [5]
Electron Saturation Velocity ($cm.s^{-1}$)	$2.6x10^{7}$	$2.5x10^{7}$ [9]
Hole Saturation Velocity ($cm.s^{-1}$)	$6.6x10^{6}$ [5]	$4.9x10^{6}$

Table III
Mobility Model Parameters

Electrons			Holes		
Parameter	**InP**	**$In_{0.47}Ga_{0.53}As$**	**Parameter**	**InP**	**$In_{0.47}Ga_{0.53}As$**
μ_{max} ($cm^2.V^{-1}.sec^{-1}$)	4917[5, 6]	11599[5, 6]	**μ_{max} ($cm^2.V^{-1}.sec^{-1}$)**	151[5, 6]	331[5, 6]
μ_{min} ($cm^2.V^{-1}.sec^{-1}$)	300[5, 6]	3372[5, 6]	**μ_{min} ($cm^2.V^{-1}.sec^{-1}$)**	20[5, 6]	75[5, 6]
N_C (cm^{-3})	$6.4x10^{17}$ [5, 6]	$8.9x10^{16}$ [5, 6]	**N_V (cm^{-3})**	$1x10^{17}$ [5, 6]	$1x10^{18}$ [5, 6]
α	0.46[5, 6]	0.76[5, 6]	**α**	0.96[5, 6]	1.37[5, 6]

4. Result and Discussion

Simulated and measured common-emitter current-voltage (*I-V*) characteristics of an SHBT with an emitter area of $5\times5\mu m^2$ are shown in Figure 1. Unlike Silicon Bipolar transistors, an offset in turn-on voltage (V_{ceo}) is observed in the SHBT *I-V* characteristics curves because of the difference in voltages turn-on of the base-emitter (Heterojunction) diode and base-collector (Homojunction) diodes. The key factor in determining the collector-emitter offset voltage and thus the saturation voltage is the potential spike in the base-emitter region. A higher turn-on voltage offset than expected was observed in the device measured and this was investigated by simulating the effect of the suspected diffusion of the p-type doping (Beryllium) from the base into the spacer layer. The relationship between the p-type doped spacer layer and its effect on the turn-on voltage is shown in Figure 2. As expected, the spacer layer between base and emitter is no longer acting as an intrinsic layer (~n-type 5×10^{14} cm^{-3}) but is rather doped p-type to a magnitude of $5\times10^{18}cm^{-3}$. This enhances the spike in the base-emitter conduction band region and thus increases the turn-on voltage to 150mV and gain to 90, as shown in Figure 1 and Figure 4.

An intrinsic spacer layer (~n-type 5×10^{14} cm^{-3}) in the simulations has demonstrated a turn-on voltage offset of 74mV, however this also results in a decrease in the gain of the device by 15% because of an increase in the recombination in the narrow-bandgap spacer region, as shown in Figure 3. Thus, there is a trade-off between the turn-on voltage and the gain of the device. For digital applications, a low turn-on and thus low saturation voltage is more important than very high gain as it lowers the overall power consumption of the device.

In order to exhibit high gain as well as low emitter collector voltages, the epi-layer structure needs to be altered to a Double Heterojunction Bipolar Transistor (DHBT) [3]. This introduces a heterojunction in the base-collector region similar to the base-emitter heterojunction and thus decreases the turn-on voltage. DHBT also offers high voltage breakdown of 8 Volts [3] because of low impact ionization as compared to SHBT which offers 4.5 Volts. The effects of the impact ionization are demonstrated in the simulations and agreed very well with the measured data.

Another improvement that can be considered is to introduce another spacer layer between base and collector layer. This will increase the base-collector diode turn-on and thus will lead to a decrease in the difference of the voltages between the base-emitter diode and base-collector diode. This will result in a decrease of the turn-on voltage of the device.

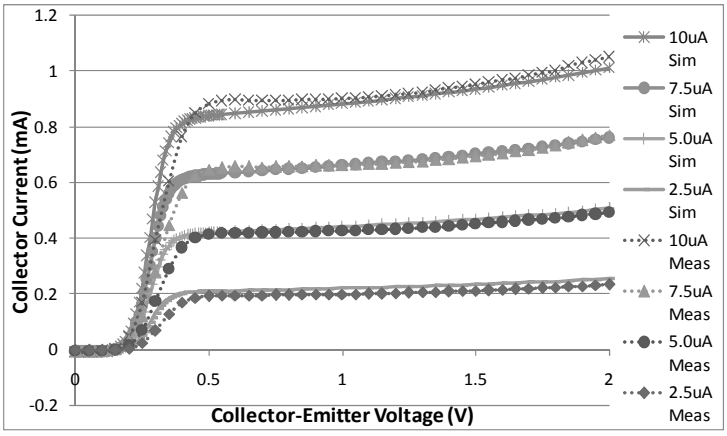


Fig. 1. Simulated and Measured I-V Characteristics Curves

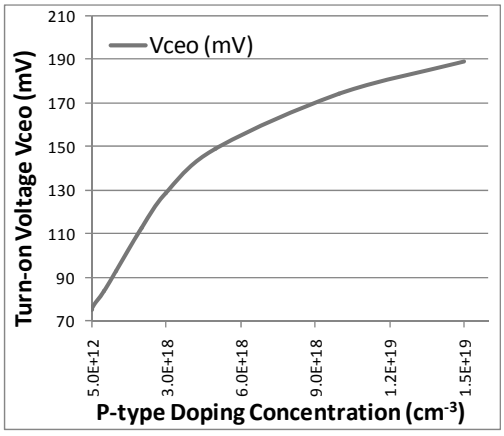


Fig. 2. Effect on turn-on voltage (V_{ceo}) by p-type doping in the spacer layer

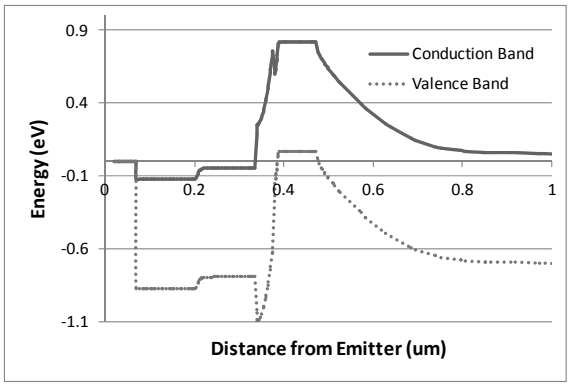


Fig. 3. SHBT Energy Band diagram with intrinsic spacer layer

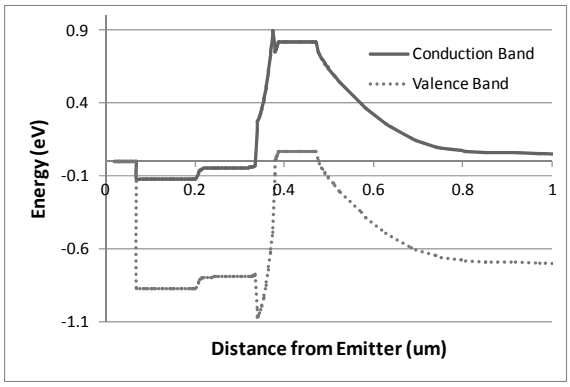


Fig. 4. SHBT Energy Band diagram without intrinsic spacer layer

5. Conclusion

Accurate physical modelling of complex InP-based HBTs has been presented which not only provides inexpensive, reliable and efficient prototyping, but also aids with the understanding of the underlying device physics. Excellent agreement between modelled and measured data is reported and physical insight into the working of the device gained. The effect of the spacer layer on the turn-on voltage and energy band diagram is studied. Further work on extending the DC simulations to RF simulations of HBTs is in progress.

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